CLAIMS

What is claimed is:

1. A cross point memory, comprising:

a substrate having a deposition face;

a memory array that includes a plurality of memory cells, wherein at least a portion of the memory cell is formed using high temperature processing at a first temperature;

a bottom refractory metal layer that has a melting point above the first temperature, parallel to the deposition face of the substrate, patterned into bottom conductive array lines; and

a top metal layer, parallel to the deposition face of the substrate, patterned into top conductive array lines such that a memory cell may be at least partially defined by the intersection of a bottom conductive array line and a top conductive array line, the memory cell capable of being programmed by application of voltages on the bottom conductive array line and the top conductive array line.

2. The cross point memory of claim 1, wherein the resistance of the memory cells can be reversibly programmed to different values.

3. The cross point memory of claim 1, wherein the memory cells include a conductive metal oxide.

4. The cross point memory of claim 1, wherein the memory cells includes a crystalline or poly-crystalline material.

5. The cross point memory of claim 1, wherein the top metal layer is not a refractory metal.

6. The cross point memory of claim 5, wherein the top metal layer is copper or an aluminum alloy.

7. The cross point memory of claim 1, wherein the bottom refractory metal layer is tungsten, molybdenum or tantalum.

8. The cross point memory of claim 1, wherein the bottom refractory metal layer has a melting point of at least 700C.

9. The cross point memory of claim 1, wherein the bottom refractory metal layer is stable at 600C.

10. The cross point memory of claim 1, wherein each of the memory cells further include:

a multi-resistive state element; and

an electrode that electrically connects the multi-resistive state element to a bottom conductive array line.

11. The cross point memory of claim 10, wherein the electrode includes a barrier layer, whereby inter-metal and oxygen diffusion is limited by the barrier layer during the memory cell formation.

12. The cross point memory of claim 11, wherein the barrier layer includes either titanium or titanium nitride.

13. The cross point memory of claim 11, wherein the barrier layer is a binary nitride.

14. The cross point memory of claim 11, wherein the barrier layer is a ternary nitride.

15. The cross point memory of claim 1, wherein the electrode includes a sacrificial layer, whereby the sacrificial layer acts as an oxygen barrier layer by reacting with oxygen while remaining electrically conductive.

16. The cross point memory of claim 15, wherein the sacrificial layer is a ternary oxide.

17. The cross point memory of claim 16, wherein the ternary oxide is ruthenium tantalum oxide, ruthenium titanium oxide, iridium tantalum oxide or iridium titanium oxide.

18. The cross point memory of claim 15, wherein the sacrificial layer is a ternary nitride.

19. The cross point memory of claim 18, wherein the ternary nitride is ruthenium tantalum nitride, ruthenium titanium nitride, iridium tantalum nitride or iridium titanium nitride.

20. The cross point memory of claim 10, wherein the electrode includes a noble metal.

21. The cross point memory of claim 10, wherein the electrode includes a conductive metal oxide such as strontium ruthenate, lanthanum nickelate or iridium oxide.

22. The cross point memory of claim 1, further comprising:

refractory interconnect metal layers in-between the substrate and the bottom refractory metal layers.

23. The cross point memory of claim 1, further comprising:

interconnect metal layers above the top metal layer.

24. The cross point memory of claim 1, wherein there are at least 2 memory arrays, whereby the at least 2 memory arrays are stacked upon one another.

25. A memory, comprising:

a substrate;

a memory array that includes a plurality of memory cells, each memory cell including a multi-resistive state element, the multi-resistive state element being above the substrate and being formed with a high-temperature fabrication process at a high temperature;

a plurality of conductive lines beneath the multi-resistive state element, the plurality of conductive being stable at the high temperature; and

a plurality of conductive lines above the multi-resistive state element.

26. The memory of claim 25, wherein the plurality of conductive lines above the multi-resistive state element are not stable at the high temperature.

27. The memory of claim 25, wherein the multi-resistive state element is re-writeable.

28. The memory of claim 25, wherein a plurality of electrodes that are stable at the high temperature are formed beneath the multi-resistive state element.

29. The memory of claim 25, wherein each of the plurality of electrodes includes a barrier layer.

30. The memory of claim 25, wherein each of the plurality of electrodes includes an adhesion layer.

31. The memory of claim 25, wherein each of the plurality of electrodes includes a sacrificial layer.

32. The memory of claim 25, wherein a plurality of contact plugs that are stable at the high temperature are formed beneath the multi-resistive state element.

33. A memory, comprising:

a substrate;

a plurality of circuits on the substrate;

a plurality of x-direction lines in a first metal layer parallel to the substrate, with the x-direction lines oriented in one direction;

a plurality of y-direction lines in a second metal layer above the first metal layer, with the y-direction lines oriented in a different direction as the x-direction lines, and crossing the x-direction lines; and

a plurality of memory plugs located substantially at the intersections of the x-direction lines and y-direction lines, and in-between the first and second metal layers;

wherein the memory plugs have at least one layer that requires a minimum temperature for fabrication;

the first metal layer is a metal with a melting point above the minimum temperature required for fabrication; and

the second metal layer is a metal that is not stable at the minimum temperature required for fabrication.

34. The memory of claim 33, wherein:

the first metal is a refractory metal.

35. The memory of claim 33, wherein:

the second metal is not capable of sustaining processing temperature above 450C.

36. The memory of claim 33, wherein:

the second metal is an aluminum alloy.

37. The memory of claim 33, wherein:

the second metal is copper.

38. The memory of claim 33, further comprising:

at least one metal layer placed in-between the first metal layer and the substrate,

wherein the at least one metal layer placed in-between the first metal layer and the substrate is tungsten.

39. The memory of claim 33, further comprising:

at least one electrode in each memory plug,

wherein the at least one electrode includes a noble metal.

40. The re-writable memory of claim 39, wherein:

the at least one electrode includes iridium, platinum or gold.

41. The re-writable memory of claim 33, further comprising:

at least one electrode in each memory plug;

wherein the at least one electrode includes a conductive metal oxide.

42. The re-writable memory of claim 41, wherein the at least one electrode includes strontium ruthenate, lanthanum nickelate or iridium oxide.

43. The re-writable memory of claim 33, wherein the memory plugs each include:

a multi-resistive state material;

a non-ohmic device;

an electrode that electrically connects the multi-resistive state element to the non-ohmic device;

an electrode that electrically connects the memory plug to an x-direction line; and

an electrode that electrically connects the memory plug to a y-direction line.

44. A method of manufacturing a memory comprising:

providing a semiconductor substrate;

forming a bottom plurality of layers that are stable at a first temperature;

forming a multi-resistive state element layer at the first temperature after the bottom plurality of layers are formed; and

forming a top plurality of layers after the multi-resistive state element layer is formed, wherein at least one of the layers in the top plurality of layers is not stable at the first temperature.

45. The cross point memory of claim 24, wherein one of the memory arrays is a topmost memory array, and all of the metal layers below the topmost memory array are refractory metal layers and at least one metal layer above the topmost memory layer is not a refractory metal layer.